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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of

TAKAFUJI et al — Atty. Ref.: 1035-501

Serial No. 10/802,735 — Group: 2811

Filed: March 18, 2004 — Examiner:

For: SEMICONDUCTOR DEVICE AND METHOD OF MANUFACTURING THE SAME

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Commissioner for Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Further to applicants' Information Disclosure Statement of June 7, 2004, applicants herewith submit a corrected Form PTO-1449 (i.e., the page numbers of the Tong et al reference and the date of the Vandooren et al reference has been corrected).

Respectfully submitted,
NIXON & VANDERHYE P.C.

June 25, 2004

By: _____
H. Warren Burnam, Jr.
Reg. No. 29,366

HWB:lsh
1100 North Glebe Road, 8th Floor
Arlington, VA 22201-4714
Telephone: (703) 816-4000
Facsimile: (703) 816-4100

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INFORMATION DISCLOSURE CITATION

(Use several sheets if necessary)

ATTY. DOCKET NO.	SERIAL NO.
1035-501	10/802,735
APPLICANT	
TAKAFUJI et al	
FILING DATE	**GROUP**
March 18, 2004	2811

U.S. PATENT DOCUMENTS

*EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		8-262474 A	10-1996	JP			partial	
		7-235651 A	9-1995	JP			partial	
		93/15589 A1	8-1993	WO				

OTHER DOCUMENTS (including Author, Title, Date, Pertinent pages, etc.)

		Salerno et al, "Single Crystal Silicon AMLCDs", Conference Record of the 1994 International Display Research Conference (IDRC) (1994), pp. 39-44
		Tong et al, "Semiconductor Wafer Bonding: Science and Technology", John Wiley & Sons, Inc., New York, 1999, pp. 8-11, 48-55, 58-65, 108 and 109
		Warner et al, "Low-Temperature Oxide-Bonded Three-Dimensional Integrated Circuits", 2002 IEEE International SOI Conference, October 2002, pp. 123-125
		Allen et al, "SOI Uniformity and Surface Smoothness Improvement Using GCIB Processing", 2002 IEEE International SOI Conference, October 2002, pp. 192-193
		Matsumoto et al, "70 nm SOI-CMOS of 135 GHz f_{max} with Dual Offset-Implanted Source-Drain Extension Structure for RF/Analog and Logic Applications", International Electron Device Meeting, December 2001, pp. 219-222
		Vandooren et al, "Scaling Assessment of Fully-Depleted SOI Technology at the 30nm Gate Length Generation", 2002 IEEE international SOI Conference Proceedings, October 2002, pp. 25-27

*Examiner		Date Considered	

Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to application.

Form PTO-FB-A820 (Also PTO-1449)